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(54) Method for selectively forming semiconductor regions

Verfahren zur selektiven Herstellung von Halbleitergebieten

Procédé de formation sélective de régions semi-conductrices

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(73) Proprietor: **MOTOROLA, INC.**
Schaumburg, IL 60196 (US)

(72) Inventors:
- **Steele, John W.**
  Chandler, Arizona 85224 (US)
- **De Fresart, Edouard**
  Tempe , Arizona 85284 (US)
- **Theodore, David N.**
  Mesa, Arizona 85213 (US)

(74) Representative:
Hudson, Peter David et al
Motorola,
European Intellectual Property,
Midpoint,
Alencon Link
Basingstoke, Hampshire RG21 7PL (GB)

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Description

Background of the Invention

[0001] This invention relates, in general, to semiconductor devices, and more particularly to a method for selectively forming semiconductor regions on semiconductor substrates.

[0002] Methods for selectively forming semiconductor regions have been reported in the past. For the selective deposition of silicon, typically a patterned semiconductor wafer having exposed oxide regions and exposed silicon regions is placed in a chemical vapor deposition (CVD) reactor and exposed to elevated temperature and a chlorine containing silicon source-gas ($SiCl_xH_y$) and hydrogen. Also, under certain conditions, hydrogen chloride (HCl) gas is used with the chlorine containing silicon source-gas and hydrogen.

[0003] In general, by controlling the temperature and pressure of the reactor and the concentrations of the chlorine and silicon sources, the process conditions are such that single-crystal silicon regions form in the exposed silicon regions. These conditions also prevent the build up of polysilicon on the exposed oxide region resulting in the selective formation of single-crystal silicon regions.

[0004] Another reported method involves using germane (GeH_4) in place of or in addition to HCl. Under appropriate process conditions, single-crystal silicon or single-crystal silicon-germanium regions form on the exposed silicon regions. The presence of germane competes with the silicon source for nucleation sites on the exposed oxide regions preventing silicon or silicon-germanium from forming on the exposed oxide regions.

[0005] An article entitled "Selective silicon epitaxial growth by LPCVD using silane" by G.J. Parker and C.M.K. Starbuck, in Electronics Letters, vol. 26, No. 13 (21.06.1990), Stevenage, Herts, GB, pages 831 to 832, discloses a method for selective silicon epitaxial growth using 100% silane. After a hydrogen bake step at 950°C, silicon wafers having oxide islands were exposed to 100% silane at a total pressure of 1 mbar and a temperature of 950°C to selectively grow silicon regions. After deposition, the silicon wafers were again exposed to hydrogen at 950°C before being unloaded. PCT application no. WO-A-91/03834 discloses a method for selectively depositing materials on substrates without depositing the materials on a adjacent masking layer. Both these techniques avoid the growth of material on masking layers (i.e. oxides) while growing material on exposed portions of the substrate material.

[0006] These selective growth techniques have several problems. For example, both of the above techniques are sensitive to the ratio of exposed silicon to exposed oxide. This is often termed "load dependent" meaning that as the amount of exposed silicon on a semiconductor wafer increases thereby decreasing the amount of exposed oxide, the thickness uniformity of selectively formed silicon regions across the wafer decreases. Also, the above techniques are sensitive to the characteristics of the exposed passivation regions. Different passivation types such as atmospherically grown oxides, deposited oxides and deposited nitrides require the manufacturer to adjust and fine tune the selective epitaxial growth process parameters depending upon the types of passivation films present on the wafer. This significantly impacts manufacturing throughput and cost. In addition, the above techniques are susceptible to faceting defects.

[0007] Thus, a need exists for a selective epitaxial growth process that is not load dependent, that does not require a manufacturer to make process adjustments depending upon the type of exposed passivation layer present, and that is less susceptible to faceting defects.

Summary of the Invention

[0008] In accordance with the present invention there is provided a method for selectively forming semiconductor regions as recited in claim 1 of the accompanying claims.

Brief Description of the Drawings

[0009]

FIG. 1 illustrates a process flow diagram in accordance with the present invention;

FIGS. 2-5 illustrate highly enlarged cross-sectional views of one embodiment according to the present invention; and

FIGS. 6-13 illustrate highly enlarge cross-sectional views of a second embodiment according to the present invention.

Detailed Description of the Drawings

[0010] Generally, the present invention relates to a method for selectively forming semiconductor regions using chemical vapor deposition (CVD) techniques. The method is suitable for selectively forming semiconductor regions using semiconductor source-gases that are substantially absent halogens. The term substantially absent halogens means the presence of halogens in the source-gas is below trace amounts. Examples of such source-gases include silane, di-silane, and germane.

[0011] The method is used to selectively form semiconductor regions including silicon, silicon-germanium, carbon-doped silicon, or carbon-doped silicon-germanium for example. The selectively formed regions may be single-crystalline, amorphous or polycrystalline. In addition, the selectively formed regions may be doped p-type or n-type. Furthermore, the method is used to selectively form multiple layer structures. The method is suitable for forming isolated regions for fabricating semiconductor devices.

[0012] The present invention can be more fully described with reference to FIGS. 1-13. In a preferred embodiment of a method for selectively forming semiconductor regions, an atmospheric pressure chemical vapor deposition reactor (APCVD) or a reduced pressure chemical vapor deposition (RPCVD) reactor (hereinafter, CVD reactor) having the capability of rapid thermal ramp rates is provided as indicated by block 3 of the process flow diagram shown in FIG. 1. The CVD reactor includes a plurality of source-gas feed lines for hydrogen, the semiconductor source-gases, and dopant gases such as arsine, phosphine, and diborane. Individuals skilled in the art are aware of many suitable CVD reactors such as an ASM Epsilon 2e Rp, an Applied Materials 7810, and the like.

[0013] To prepare the CVD reactor for chemical vapor deposition, a helium leak check is performed on the CVD reactor as shown by block 4 of FIG. 1. The CVD reactor must pass a helium leak check of less than approximately 1.33×10^{-6} Pa (1×10^{-8} mm Hg). A CVD reactor that meets this requirement ensures that contaminants such as oxygen and water vapor do not enter the reactor and form an oxide layer on an exposed semiconductor substrate over which a blanket semiconductor layer will be formed. In addition, passing the helium leak check ensures that when highly reactive gases are used during processing, potential adverse reactions are avoided. A CVD reactor failing the helium leak test must be repaired and retested until it passes as indicated in the feedback portion (block 5) of FIG. 1. A CVD reactor that passes the helium leak test is called an ultra-clean reactor.

[0014] The helium leak check may be performed, for example, by connecting a turbo-helium leak detector to the CVD reactor, coating an exterior portion of the fillings connected to the reactor with helium, and checking for the presence of helium with the CVD reactor. Helium leak checks and procedures for performing helium leak checks are well known to those skilled in the art.

[0015] In the preferred embodiment, a patterned substrate having exposed regions of semiconductor material and passivation regions comprising exposed oxide is placed in a suitable CVD reactor chamber, for example, an ASM Epsilon 2e Rp. This procedure is illustrated in block 6 of FIG. 1. The passivation regions comprise an exposed oxide layer where the oxide preferably is either a thermal oxide or a densified deposited oxide. Alternatively, the passivation regions may further comprise a non-oxide layer under the exposed oxide layer such as a nitride layer, a high-temperature metal layer such as titanium, or a high-temperature metal-nitride layer such as titanium-nitride for example.

[0016] In addition, the semiconductor substrate may have multiple passivation regions comprised of exposed oxide layers and/or passivation regions comprised of exposed non-oxide layers such as exposed nitride layers. As will be explained below, the exposed oxide layer provides for the selective formation of semiconductor regions by the selective removal of deposited polycrystalline semiconductor material formed over the exposed oxide layer.

[0017] Preferably, the patterned substrate is cleaned, as shown in block 2 of FIG. 1, prior to placing it inside the CVD reactor chamber. In the most preferred embodiment, the patterned substrate is cleaned in a bath comprising approximately 18:1 volumes of sulfuric acid (H_2SO_4):hydrogen peroxide (H_2O_2) at approximately 100 to 120°C for 5 to 15 minutes, followed by a bath comprising approximately 50:1 volumes of H_2O:hydrofluoric acid (HF) at approximately 15 to 30°C for 1 to 5 minutes. Next the patterned substrate is cleaned in a bath comprising approximately 2.5:2.5:12 volumes of Ammonia (NH_4OH):H_2O_2:H_2O at approximately 45 to 65°C for 8 to 12 minutes, followed by a bath comprising approximately 2.5:2.5:12 volumes of hydrochloric acid (HCl):H_2O_2:H_2O at approximately 40 to 60°C for 8 to 12 minutes.

[0018] Alternatively, the patterned substrate is cleaned in-situ using, for example, a cluster tool apparatus that includes a chamber for cleaning a substrate that is separate from the CVD chamber. A gas such as hydrogen chloride gas may be used to clean the substrate and such cleaning techniques are well known to those skilled in the art.

[0019] After the patterned substrate is placed into the reactor chamber, the reactor temperature is increased, as shown in block 7 in FIG. 1, to a pre-bake temperature between 900 and 1000°C using a temperature ramp rate of approximately 20°C/sec. When a reduced pressure CVD reactor is used, the reactor is pumped down to a pressure of approximately 5.33×10^3 to 1.07×10^4 Pa (40 to 80 torr) prior to ramping the reactor to the pre-bake temperature. This pressure range is used throughout the process when a RPCVD reactor is used.

[0020] After the reactor has reached the pre-bake temperature, the patterned substrate is exposed to an atmosphere consisting essentially of hydrogen to reduce any native oxide present on the patterned substrate as a result of the pre-clean step. This process is shown as block 8 in FIG. 1. Preferably, the pre-bake atmosphere consists essentially of hydrogen and the patterned substrate is exposed to the pre-bake temperature and hydrogen atmosphere for approximately 5 minutes with a hydrogen flow-rate of approximately 20 to 200 standard liters per minute (slm). In the most preferred embodiment, the hydrogen flow-rate is approximately 100 slm.

[0021] After the pre-bake step, the CVD reactor is reduced to the semiconductor layer growth temperature of between 650 and 850°C as represented by block 9 in FIG. 1. Preferably, a ramp rate of approximately 10°C/second is used. The preferred growth temperature is between 750 and 800°C. While the reactor is ramping to the growth temperature, the semiconductor source-gas lines are purged with hydrogen.

[0022] Once the reactor chamber has reached the growth temperature and the semiconductor source-gas lines are purged, the semiconductor source-gas is introduced into the reactor chamber along with a hydrogen carrier gas having a flow-rate of approximately 20 to 200 slm with a flow-rate of 100 slm preferred. During the growth step, the atmosphere in the reactor is substantially absent the presence of halogens. Under these conditions, a blanket semiconductor film or layer is formed over the patterned semiconductor substrate as represented by block 10 of FIG. 1. Because a blanket layer is formed, the process is not load dependent, it is less sensitive to the characteristics of the exposed passivation regions, and it is less susceptible to faceting defects.

[0023] The blanket semiconductor layer comprises polycrystalline semiconductor material over the exposed oxide layer. In addition, when the patterned substrate also comprises exposed non-oxide layers such as silicon nitride, polycrystalline semiconductor material forms over the non-oxide layer. The blanket semiconductor layer further comprises single-crystal semiconductor material where the exposed semiconductor material on the patterned substrate is single-crystal semiconductor material. With a silane semiconductor source-gas, a growth temperature of approximately 750°C, and a silane flow-rate of approximately 5 slm, a growth rate of approximately 0.04 microns/minute is achieved. In addition, when a silane source-gas is used, preferably a 2% silane in hydrogen source-gas is used having a purity of 99.99999%.

[0024] In the most preferred embodiment, gas purifying filters are attached to all gas lines in order to provide ultra-dry gases and an atmosphere within the reactor chamber that is substantially absent moisture. Preferably the gas line purifying filters result in less than $5x10^{18}$ atoms/cm^3 of oxygen in the blanket semiconductor layer as measured using a secondary ion mass-spectrometer technique. Examples of such gas purifying filters include the Nanochem® Hydrogen 3000, Nitrogen 1400, and Silane IV available from Semigas Systems Inc.

[0025] During the formation of the blanket semiconductor layer, dopants such as boron, phosphorus, or arsenic may be introduced into the blanket layer by using dopant source-gases such as diborane, phosphine, or arsine. In addition, the blanket semiconductor layer may be doped with germanium using a germane source-gas and/or carbon using a propane source-gas to provide for bandgap engineered devices. When germane is used to form germanium doped silicon devices, the germane concentration is kept below $5.0x10^{20}$ atoms/cm^3 to prevent selectivity of the polycrystalline material as the blanket semiconductor layer is formed.

[0026] Once the blanket semiconductor layer reaches the desired thickness, the semiconductor source-gas and any dopant gases ar shut off from the reactor chamber and the reactor chamber and gas lines are purged with hydrogen for approximately 2 minutes. While the reactor chamber and gas lines are under purge, the reactor chamber temperature is increased to an inner-bake temperature between 900 and 1200°C using a temperature ramp rate of approximately 20°C/second as represented by block 11 in FIG. 1. During the inner-bake step, as represented by block 12 of FIG. 1, hydrogen flows into the reactor chamber at flow-rate between 20 and 200 slm with a flow-rate of 100 slm preferred.

[0027] By exposing the patterned substrate to an elevated temperature and hydrogen, the polycrystalline semiconductor material portion of the blanket layer over the previously exposed oxide layer is selectively removed leaving a remaining portion of the blanket layer that is single-crystal semiconductor material. Also, a portion of the underlying previously exposed oxide layer is removed in an amount dependent upon, among other things, time, temperature, and characteristics of the exposed oxide layer. In addition, that portion of the blanket layer that is over an exposed non-oxide layer, such as silicon nitride, is not removed. Preferably, the atmosphere in the CVD reactor during the inner-bake step consists essentially of hydrogen.

[0028] Preferably, the patterned substrate is exposed to a temperature of approximately 1100°C for an amount of time sufficient to remove the polycrystalline semiconductor material over the exposed oxide layer. It has been determined that approximately 10 seconds at approximately 1100°C is sufficient to remove approximately 100mm (1000 angstroms) of polycrystalline semiconductor material and approximately (5000 angstroms) of exposed oxide under the polycrystalline semiconductor material.

[0029] It is believed that the selective removal of the polycrystalline semiconductor material and the exposed oxide layer under the polycrystalline material results from a series of reaction steps including the surface adsorption of hydrogen on the polysilicon, the surface dissociation of hydrogen, the surface diffusion of hydrogen to the interface between the polycrystalline material and the exposed oxide, the surface reduction of silicon to produce adsorbed silicon, and the reaction of adsorbed silicon with the exposed oxide to produce volatile silicon oxide (SiO).

[0030] In an alternative embodiment, the patterned substrate is removed from the CVD reactor chamber after the blanket semiconductor layer is grown. The patterned wafer is then exposed to the elevated temperature and hydrogen using a thermal anneal system capable of providing rapid thermal ramp rates and a hydrogen atmosphere. An example of such a rapid thermal anneal system is an AST SHS2000. However, it is preferred that both the growth step and the inner-bake step take place in-situ within a CVD reactor to minimize manufacturing costs and capital investment. In addition, the in-situ process reduces the exposure of the substrate to particulates and contamination associated

with, among other things, excessive substrate handling.

[0031] FIGS. 2-5 provide cross-sectional views of an example of a process to selectively form semiconductor regions by selective removal of polycrystalline semiconductor material and exposed oxid , according to the present invention. FIG. 2 illustrates a cross-sectional view of a semiconductor substrate 21 having an oxide layer 22, a non-oxide layer 23, and an exposed oxide layer 24 formed thereon at a stage of fabrication. Non-oxide layer 23 comprises a nitride layer for example.

[0032] FIG. 3 shows semiconductor substrate 21 at a later stage of fabrication after standard photolithography techniques are used to form openings 26 and 27. Openings 26 and 27 expose portions of semiconductor substrate 21. After openings 26 and 27 are formed, substrate 21 is cleaned using the techniques described with block 2 of FIG. 1. After substrate 21 is cleaned, it is placed into a CVD reactor that passes the helium leak test as described with blocks 3-6 of FIG. 1.

[0033] FIG. 4 shows substrate 21 after a blanket layer is grown on substrate 21 as described with block 10 of FIG. 1. The blanket layer has single-crystal semiconductor regions 28 formed in openings 26 and 27 and polycrystalline regions 29 formed over exposed oxide layer 24. After the blanket layer is formed on substrate 21, substrate 21 is exposed to the high temperature and hydrogen atmosphere, as described with block 12 of FIG. 1, to selectively remove polycrystalline regions 29 and exposed oxide layer 24 leaving single-crystal semiconductor material regions 28, non-oxide layer 23, and oxide layer 22 on substrate 21 as shown in FIG. 5. The thickness of exposed oxide layer 24 is selected such that all or only a portion of exposed oxide layer 24 is removed during the inner-bake step.

[0034] FIGS. 6-13 illustrate highly enlarged cross-sectional views of a second example of a process according to the present invention. The second example uses the present invention during the fabrication of a bipolar-complementary metal-oxide semiconductor (BICMOS) device. FIG. 6 shows a cross-sectional view of a semiconductor substrate 34 having an NPN bipolar device region 36, an N-MOS device region 37, and a P-MOS device region 38 at an interim step of fabrication. Preferably, substrate 34 comprises single-crystal silicon. It is understood that dopant configuration is shown as an example only and that others are possible.

[0035] In the embodiment shown, substrate 34 is a p-type substrate having a doping concentration on the order of 2.0 to $7.0x10^{15}$ atoms/cm^3. Bipolar device region 36, N-MOS device region 37, and P-MOS device region 38 are passivated using passivation regions 51. Passivation regions 51 preferably comprise a silicon oxide, and are commonly referred to as field oxide. Methods for forming passivation regions 51 are well known in the art. Trench isolations 52 further isolate bipolar device region 36 from N-MOS device region 37 and P-MOS device region 38. Optionally, trench isolation 52 includes a polycrystalline semiconductor region 50. Polycrystalline semiconductor region 50 provides stress relieved refill for trench isolations 52. Methods for forming trench isolations 52 ar well kn wn in the art.

[0036] Bipolar device region 36 comprises an n-type buried layer region 42 having a doping concentration on the order of 0.5 to $1.0x10^{19}$ atoms/cm^3, an n-type collector region 43 having a doping concentration of 0.5 to $1.0x10^{16}$ atoms/cm^3, and an n-type deep contact region 49 having a dopant concentration on the order of 0.5 to $1.0x10^{19}$ atoms/cm^3. It is understood that other dopant ranges are applicable, depending upon the particular device requirements. Opening 41 provides access to n-type collector region 43 for later forming base and emitter regions. Methods for forming opening 41 are well known in the art.

[0037] N-MOS region 37 comprises a p-type buried layer 44 having a dopant concentration on the order of 0.1 to $1.0x10^{19}$ atoms/cm^3 and a p-type well region 46 having a dopant concentration on the order of 0.5 to $5.0x10^{16}$ atoms/cm^3. P-MOS region 38 comprises an n-type buried layer 47 having a dopant concentration on the order of 0.5 to $1.0x10^{19}$ atoms/cm^3 and an n-type well region 48 having a dopant concentration on the order of $5.0x10^{13}$ to $1.0x10^{15}$ atoms/cm^3. It is understood that other dopant ranges are applicable, depending upon the particular device requirements. Methods for forming n-type buried layer 42, n-type collector region 43, n-type deep contact 49, p-type buried layer 44, p-type well 46, n-type buried layer 47, and n-type well region 48 are well known in the art.

[0038] Substrate 34 further has patterned passivation layer 53 over N-MOS region 37 and P-MOS region 38. Preferably passivation layer 53 comprises an oxide and is on the order of 20 to 100nm (200 to 1000 angstroms) thick. Patterned passivation layer 53 protects N-MOS region 37 and P-MOS region 38 during subsequent processing to bipolar device region 36. In addition, patterned passivation layer 53 may act as a sacrificial gate oxide. Methods for forming patterned passivation layer 53 are well known in the art.

[0039] FIG. 7 shows substrate 34 at a later step in fabrication. A blanket layer comprising polysilicon regions 56 and single-crystal silicon regions 54 and 55 is formed over the surface of substrate 34. The blanket layer is formed preferably using the process set forth with blocks 2-10 of FIG. 1. Preferably, the blanket layer is not doped. If the blanket layer is doped, it is doped with boron at a dopant concentration of 1.0 to $5.0x10^{16}$ atoms/cm^3 when bipolar device region 36 comprises an NPN transistor. Single-crystal silicon region 54 acts as a buffer layer between n-type collector region 43 and base region 64, shown in FIG. 10, to account for dopant movement during subsequent high temperature processes. When the blanket layer is lightly doped with boron, the concentration of n-type deep contact 49 must be high enough to compensate for the p-type dopant in silicon region 55 during subsequent high temperature

processing. Optionally, n-type deep contact 49 is covered with an oxide during the blanket layer deposition and polysilicon regions 56 extend over the oxide above n-type deep contact 49.

[0040] FIG. 8 shows substrate 34 at a later step in fabrication. A series of passivation layers are formed over the blanket layer, the series of passivation layers preferably comprises silicon oxide layer 57, silicon nitride layer 58 and silicon oxide layer 59. Silicon oxide layer 57 is on the order of 10 to 20 nm (100 to 200 angstroms) thick, silicon nitride layer 58 is on the order of 50 to 150 nm (500 to 1500 angstroms) thick, and silicon oxide layer 59 is on the order of 10 to 300 nm (100 to 3000 angstroms) thick. Preferably, silicon oxide layer 57 is formed using low pressure chemical vapor deposition (LPCVD) and a tetraethylorthosilicate (TEOS) source, silicon nitride layer 58 is formed using either plasma enhanced CVD (PECVD) or LPCVD, and silicon oxide layer 59 is formed using LPCVD TEOS.

[0041] As shown in FIG. 9, an opening 63 is formed through a portion of silicon oxide layer 59, silicon nitride layer 58, and silicon oxide layer 57 to provide access to a portion of bipolar device region 36. Methods for forming opening 63 through silicon oxide layer 59, silicon nitride layer 58, and silicon oxide layer 57 are well known in the art.

[0042] As shown in FIG. 10, after opening 63 is formed, a blanket layer comprising polysilicon region 66 and single-crystal silicon region 64 is formed using the process set forth with blocks 2-10 of FIG. 1. Preferably, the blanket layer is doped with boron having a dopant concentration on the order of $5.0x10^{16}$ to $5.0x10^{19}$ atoms/cm^3 when bipolar region 36 is designed for an NPN transistor. Single-crystal silicon region 64 forms a remaining portion of the base of bipolar device region 36. Optionally, the blanket layer comprising regions 66 and 64 is doped with germanium to provide a heterojunction device.

[0043] As shown in FIG. 11, after the blanket layer comprising polysilicon region 66 and single-crystal silicon region 64 is formed, substrate 34 is exposed to high temperature and a hydrogen atmosphere as shown with block 12 of FIG. 1 to selectively remove portions of polysilicon layer 66 and polysilicon layer 56. Also, the exposure of substrate 34 to the high temperature and hydrogen atmosphere removes oxide layer 59 but not silicon nitride layer 58. In addition, exposure of substrate 34 to the high temperature and hydrogen atmosphere together with oxide from silicon oxide layer 57 and oxide layers 51 adjacent to single-crystal silicon regions 54 and 64 provide for the formation of openings 69 and 71 through polysilicon layers 66 and 56.

[0044] FIG. 12 shows substrate 34 at a later step in fabrication. Standard photolithography and etch processes are used to remove silicon nitride layer 58, silicon oxide layer 57, portions of polysilicon region 56, and oxide layer 53.

[0045] FIG. 13 shows bipolar device region 36 having a completed bipolar device. Oxide layer 72 is formed over the entire surface of substrate 34. Oxide layer 72 preferably comprises silicon oxide formed using LPCVD TEOS. Oxide layer 72 is patterned to allow the formation of emitter region 73. Methods for patterning oxide layer 72 and forming emitter region 73 are well known in the art. Oxide layer 72 is further patterned and contact layers 74, 76, and 77 are formed providing contact to n-type collector region 43, emitter region 73, and base regions 54 and 64 respectively. Preferably, contact layers 74, 76, and 77 comprise doped polysilicon. Methods for forming contact layers 74, 76, and 77 are well known in the art. Field effect transistor (FET) devices are then formed in N-MOS region 37 and P-MOS region in a conventional manner. Optionally, the FET devices are fabricated prior to the formation of contact layers 74, 76, and 77.

[0046] By now, it should be appreciated that there has been provided a method for selectively forming semiconductor regions. By exposing a patterned substrate having exposed regions of semiconductor material and exposed regions of oxide to a first temperature and a semiconductor source-gas and hydrogen in an atmosphere substantially absent halogens, a blanket semiconductor layer forms over the exposed regions of semiconductor material. The absence of halogens provides for the formation of the blanket semiconductor layer. Polycrystalline semiconductor material forms over the exposed regions of oxide. By further exposing the patterned substrate to a second temperature higher than the first temperature in a hydrogen atmosphere, the polycrystalline semiconductor material formed over the exposed oxide regions and the exposed oxide regions are selectively removed leaving that portion of the blanket semiconductor layer over the exposed regions of semiconductor material. Because the method uses the formation of a blanket semiconductor layer, the method is not load dependent, it does not require a manufacturer to make process adjustments depending upon the type of exposed passivation layer present, and it is less susceptible to faceting defects.

Claims

1. A method for selectively forming single crystal semiconductor regions comprising the steps of:

   placing a substrate (21,34) comprising a first region of exposed semiconductor material (26,27,43,49) and a second region of exposed oxide (24,51,53,59) into a CVD reactor (3);
   forming a blanket semiconductor layer over the first region (26 27,43,49) and the second region (24,51,53,59) by exposing the substrate (21,34) at a first temperature to a semiconductor source-gas and hydrogen in an atmosphere in which halogens and moisture are substantially absent,

wherein that portion of the blanket semiconductor layer formed over the second region (24,51,53,59) comprises polycrystalline semiconductor material (29,56,66) and that portion of the blanket semiconductor layer formed over the first region is single crystal; and

exposing the substrate (21,34) to a second temperature higher than the first temperature and to hydrogen to selectively remove the polycrystalline semiconductor material (29,56,66) over the second region (24,51,53,59) while leaving a remaining portion (28,53,55,64) of the blanket semiconductor layer

over the first region (26,27,43,49).

2. The method of claim 1 further comprising the steps of:

cleaning the substrate (21,34) prior to placing the substrate (21,34) into the CVD reactor (3);
purging the CVD reactor (3) of the semiconductor source-gas before the step of exposing the substrate (21,34) to the second temperature; and
exposing the substrate (21,34) to a third temperature that is higher than the first temperature and less than or equal to the second temperature in an atmosphere consisting essentially of hydrogen prior to the step of exposing the substrate (21,34) to the first temperature, and the semiconductor source-gas and hydrogen.

3. The method of claim 2 wherein the step of exposing the substrate (21,34) to a third temperature comprises exposing the substrate (21,34) to a temperature of approximately 900°C, and wherein the step of exposing the substrate (21,34) to the semiconductor source-gas and hydrogen while at the first temperature comprises exposing the substrate (21,34) to a silane source-gas and hydrogen while at a temperature between 650°C and 850°C, and wherein the step of exposing the substrate (21,34) to a second temperature comprises exposing the substrate (21,34) to a temperature between 900°C and 1200°C.

4. The method of claim 3 wherein the steps of exposing the substrate (21,34) to the temperature of approximately 900°C, exposing the substrate (21,34) to the silane source-gas and hydrogen while at the temperature between 650°C and 850°C, and exposing the substrate (21,34) to the temperature between 900°C and 1200°C take place without exposure of the substrate (21,34) to an ambient outside of the CVD reactor (3).

5. The method of claim 1 wherein the step of exposing the substrate (21,34) to the second temperature takes place in a rapid thermal anneal system.

6. The method of claim 1 wherein the step of forming the blanket semiconductor layer includes exposing the substrate to silane, germane, and hydrogen.

7. The method of claim 1 further comprising the step of forming a semiconductor device using the remaining portion of the blanket layer.

Patentansprüche

1. Verfahren zur selektiven Herstellung von einkristallinen Halbleiterbereichen, umfassend die folgenden Verfahrensschritte:

Plazieren eines Substrats (21, 34), umfassend einen ersten Bereich mit freigelegtem Halbleitermaterial (26, 27, 43, 49) und einen zweiten Bereich mit freigelegtem Oxid (24, 51, 53, 59), in eine CVD-Reaktionsvorrichtung oder einen CVD-Reaktor (3);

Bilden einer Halbleiterdeckschicht über dem ersten Bereich (26, 27, 43, 49) und dem zweiten Bereich (24, 51, 53, 59) durch Aussetzens des Substrats (21, 34) mit einem Halbleiterquellengas und Wasserstoff bei einer ersten Temperatur in einer Atmosphäre, in der Halogene und Feuchtigkeit im wesentlichen nicht vorhanden sind, wobei der Teil der Halbleiterdeckschicht, der über dem zweiten Bereich (24, 51, 53, 59) gebildet ist, ein polykristallines Halbleitermaterial (29, 56, 66) umfaßt, und der Teil der Halbleiterdeckschicht, der über dem ersten Bereich gebildet ist, ein Einkristall ist oder einkristallin ist; und

Aussetzen des Substrats (21, 34) mit einer zweiten Temperatur, die höher als die erste Temperatur ist, und mit Wasserstoff, um das polykristalline Halbleitermaterial (29, 56, 66) über dem zweiten Bereich (24, 51, 53, 59) selektiv zu entfernen, während ein verbleibender Teil (28, 53, 55, 64) der Halbleiterdeckschicht über dem ersten Bereich (26, 27, 43, 49) verbleibt.

2. Verfahren nach Anspruch 1, gekennzeichnet durch die folgenden weiteren Schritte:

Reinigen des Substrats (21, 34) vor Plazieren des Substrats (21, 34) in die CVD-Reaktionsvorrichtung (3) oder den CVD-Reaktor (3);

Entleeren der CVD-Reaktionsvorrichtung (3)

oder des CVD-Reaktors (3) von dem Halbleiterquellengas vor dem Schritt des Aussetzens des Substrats (21, 34) mit der zweiten Temperatur; und

Aussetzen des Substrats (21, 34) mit einer dritten Temperatur, die höher als die erste Temperatur und kleiner oder gleich ist als die zweite Temperatur, und zwar in einer Atmosphäre, die im wesentlichen aus Wasserstoff besteht, und zwar vor dem Schritt des Aussetzens des Substrats (21, 34) mit einer ersten Temperatur und dem Halbleiterquellengas und Wasserstoff.

3. Verfahren nach Anspruch 2, wobei der Schritt des Aussetzens des Substrats (21,34) mit einer dritten Temperatur das Aussetzen des Substrats (21, 34) mit einer Temperatur von ungefähr 900° C umfaßt, und wobei der Schritt des Aussetzens des Substrats (21, 34) mit der ersten Temperatur mit dem Halbleiterquellengas und dem Wasserstoff das Aussetzen des Substrats (21, 34) mit einem Silan-Quellengas und Wasserstoff bei einer Temperatur zwischen 650° C und 850° C umfaßt, und wobei der Schritt des Aussetzens des Substrats (21, 34) mit einer zweiten Temperatur das Aussetzen des Substrats (21, 34) mit einer Temperatur zwischen 900° C und 1200° C umfaßt.

4. Verfahren nach Anspruch 3, wobei die Schritte des Aussetzens des Substrats (21, 34) mit einer Temperatur von ungefähr 900° C, das Aussetzen des Substrats (21, 34) mit dem Silan-Quellengas und Wasserstoff bei einer Temperatur zwischen 650° C und 850° C, und das Aussetzen des Substrats (21, 34) mit einer Temperatur zwischen 900° C und 1200° C ohne Aussetzen des Substrats (21, 34) mit einer Außenumgebung der CVD-Reaktionsvorrichtung (3) oder des CVD-Reaktors (3) stattfindet.

5. Verfahren nach Anspruch 1, wobei der Schritt des Aussetzens des Substrats (21, 34) mit einer zweiten Temperatur in einem Schnellwarmbehandlungssystem oder Schnellheizausheilsystem (rapid thermal anneal system) stattfindet.

6. Verfahren nach Anspruch 1, wobei der Schritt des Bildens der Halbleiterdeckschicht das Aussetzen des Substrats mit Silan, Germaniumwasserstoff und Wasserstoff beinhaltet.

7. Verfahren nach Anspruch 1, gekennzeichnet durch den weiteren Schritt des Bildens einer Halbleitereinrichtung, wobei der verbleibende Teil der Deckschicht verwendet wird.

Revendicati ns

1. Procédé permettant de former sélectivement des régions semiconductrices monocristallines, comprenant les opérations suivantes :

   placer dans un réacteur de dépôt chimique en phase vapeur, ou réacteur CVD, (3), un substrat (21, 34) comprenant une première région de matière semiconductrice exposée (26, 27, 43, 49) et une deuxième région d'oxyde exposé (24, 51, 53, 59) ;
   former une couche semiconductrice de couverture sur la première région (26, 27, 43, 49) et la deuxième région (24, 51, 53, 59) en exposant le substrat (21, 34), à une première température, à un gaz source de semiconducteur et à de l'hydrogène dans une atmosphère dans laquelle halogènes et humidité sont pratiquement absents, où la partie de la couche semiconductrice de couverture formée sur la deuxième région (24, 51, 53, 59) comprend une matière semiconductrice polycristalline (29, 56, 66) et la partie de la couche semiconductrice de couverture formée sur la première région est monocristalline ; et
   exposer le substrat (21, 34) à une deuxième température plus élevée que la première température et à de l'hydrogène afin de retirer sélectivement la matière semiconductrice polycristalline (29, 56, 66) sur la deuxième région (24, 51, 53, 59) tout en laissant une partie restante (28, 53, 55, 64) de la couche semiconductrice de couverture sur la première région (26, 27, 43, 49).

2. Procédé selon la revendication 1, comprenant en outre les opérations suivantes :

   nettoyer le substrat (21, 34) avant de le placer dans le réacteur CVD (3) ;
   purger le réacteur CVD (3) du gaz source de semiconducteur avant l'opération d'exposition du substrat (21, 34) à la deuxième température ; et
   exposer le substrat (21, 34) à une troisième température, qui est supérieure à la première température et inférieure ou égale à la deuxième température, dans une atmosphère consistant principalement en hydrogène avant l'opération d'exposition du substrat (21, 34) à la première température et au gaz source de semiconducteur et à l'hydrogène.

3. Procédé selon la revendication 2, où l'opération d'exposition du substrat (21, 34) à une troisième température comprend l'exposition du substrat (21, 34) à une température d'environ 900°C, où l'opéra-

tion d'exposition du substrat (21, 34) au gaz source de semiconducteur et à de l'hydrogène tandis qu'il se trouve à la première température comprend l'exposition du substrat (21, 34) à un gaz source d silane et à de l'hydrogène tandis qu'il se trouve à une température comprise entre 650°C et 850°C, et où l'opération d'exposition du substrat (21, 34) à une deuxième température comprend l'exposition du substrat (21, 34) à une température comprise entre 900°C et 1200°C.

4. Procédé selon la revendication 3, où les opérations consistant à exposer le substrat (21, 34) à une température d'environ 900°C, à exposer le substrat (21, 34) au gaz source de silane et à de l'hydrogène tandis qu'il se trouve à la température comprise entre 650°C et 850°C et à exposer le substrat (21, 34) à la température comprise entre 900°C et 1200°C ont lieu sans exposition du substrat (21, 34) à l'atmosphère ambiante extérieure au réacteur CVD (3).

5. Procédé selon la revendication 1, où l'opération d'exposition du substrat (21, 34) à la deuxième température a lieu dans un système de recuit thermique rapide.

6. Procédé selon la revendication 1, où l'opération de formation de la couche semiconductrice de couverture comporte l'exposition du substrat à du silane, du germane, c'est-à-dire de l'hydrure de germanium, et à de l'hydrogène.

7. Procédé selon la revendication 1, comprenant en outre l'opération consistant à former un dispositif à semiconducteur en utilisant la partie restante de la couche de couverture.

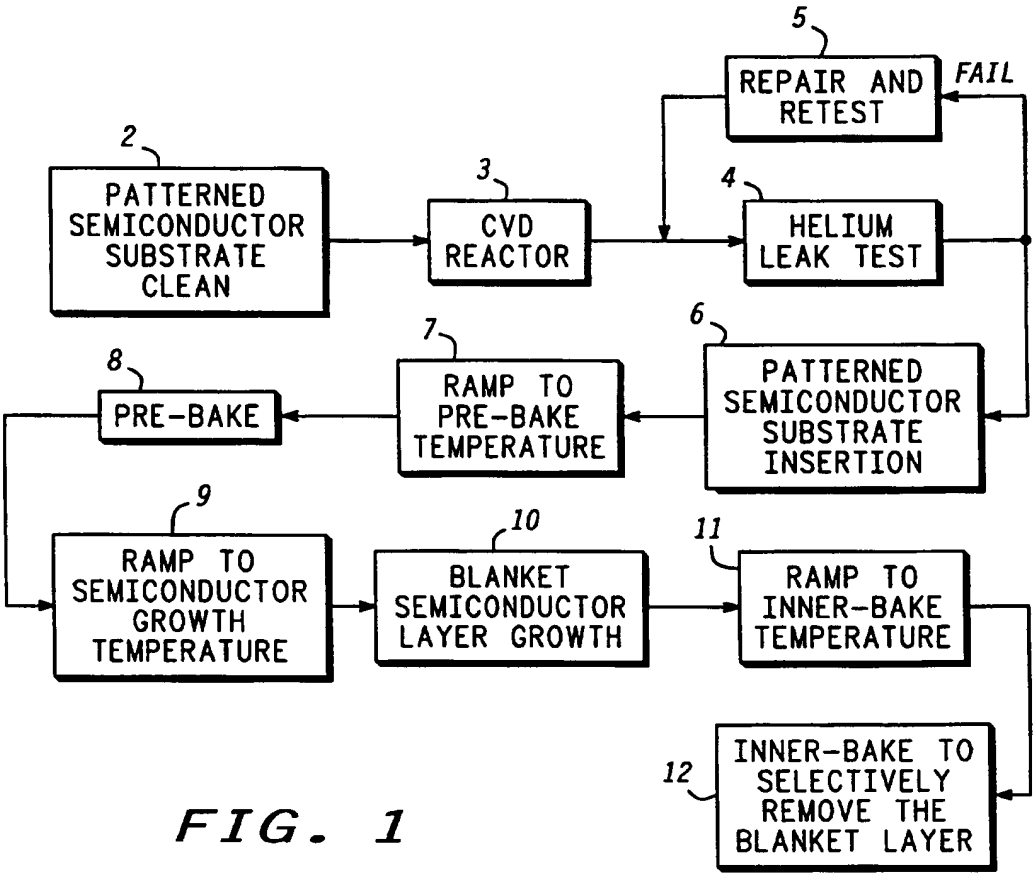

2
PATTERNED SEMICONDUCTOR SUBSTRATE CLEAN
3
CVD REACTOR
4
HELIUM LEAK TEST
5
REPAIR AND RETEST
FAIL
6
PATTERNED SEMICONDUCTOR SUBSTRATE INSERTION
7
RAMP TO PRE-BAKE TEMPERATURE
8
PRE-BAKE
9
RAMP TO SEMICONDUCTOR GROWTH TEMPERATURE
10
BLANKET SEMICONDUCTOR LAYER GROWTH
11
RAMP TO INNER-BAKE TEMPERATURE
12
INNER-BAKE TO SELECTIVELY REMOVE THE BLANKET LAYER

FIG. 1

FIG. 2

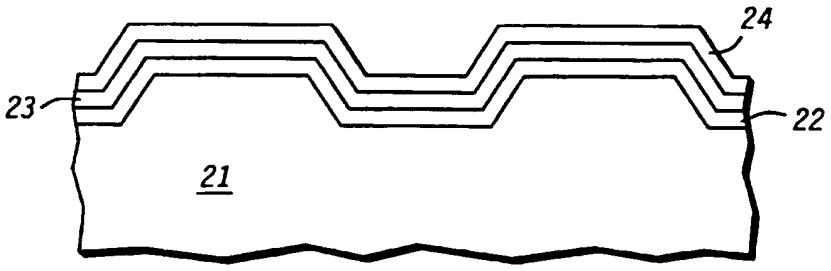


FIG. 3

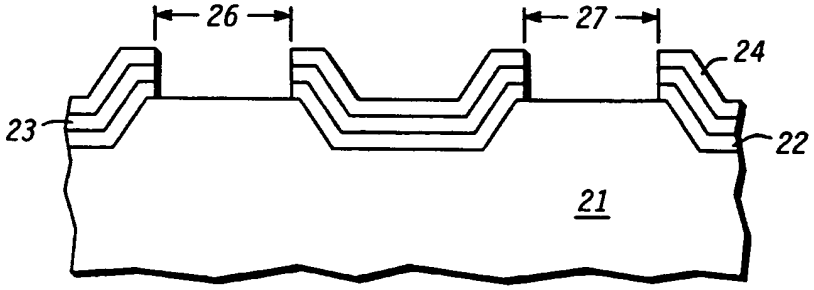


FIG. 4

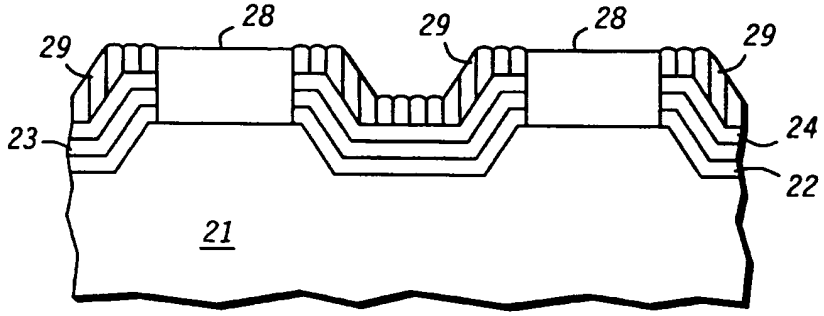
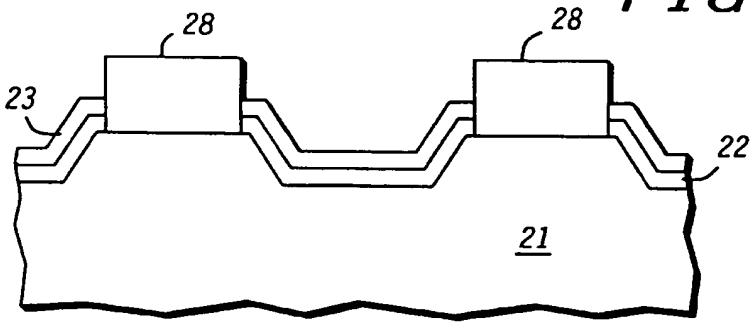


FIG. 5



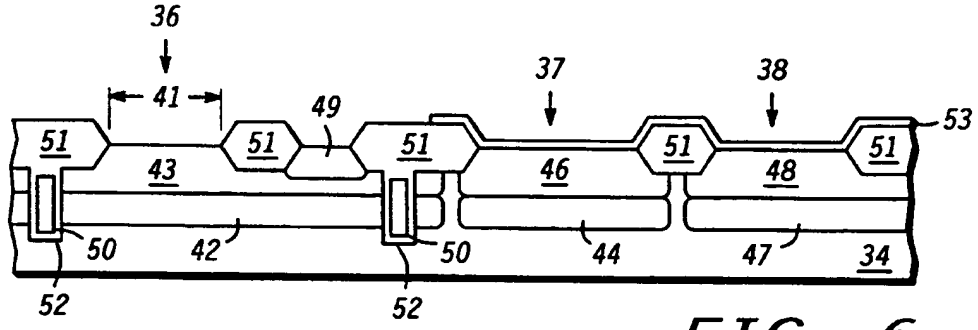


FIG. 6

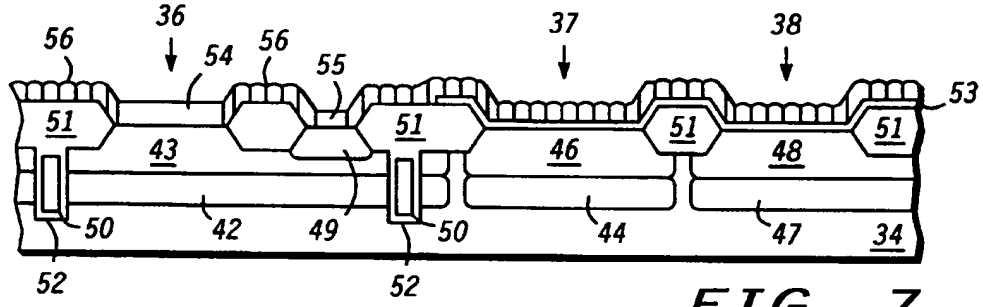


FIG. 7

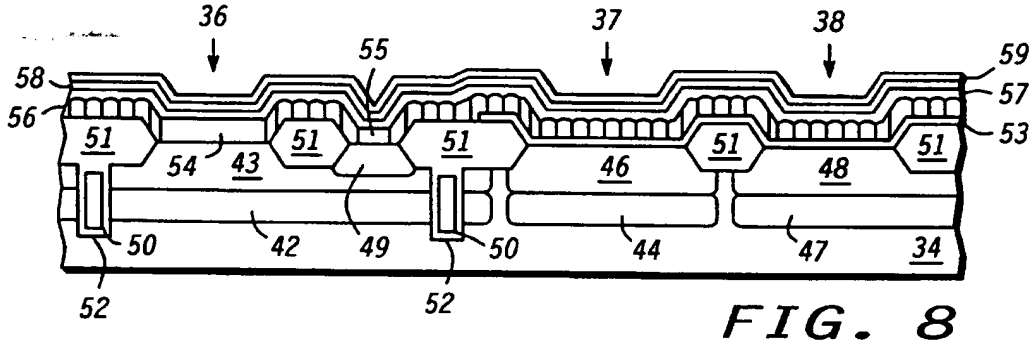


FIG. 8

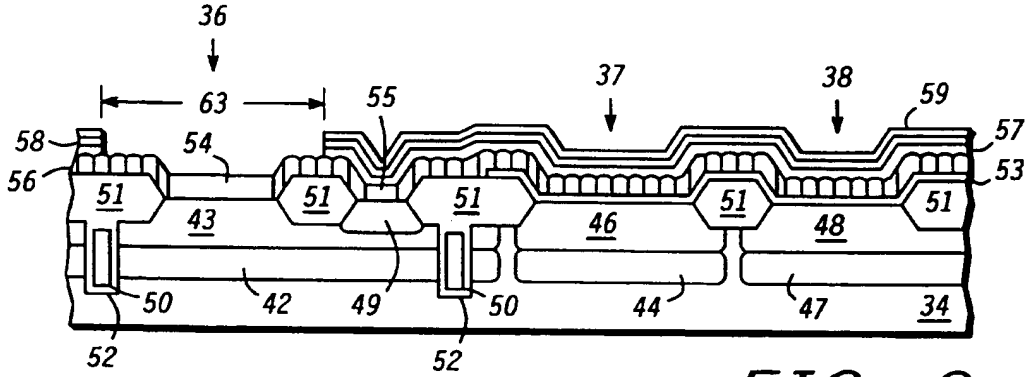


FIG. 9

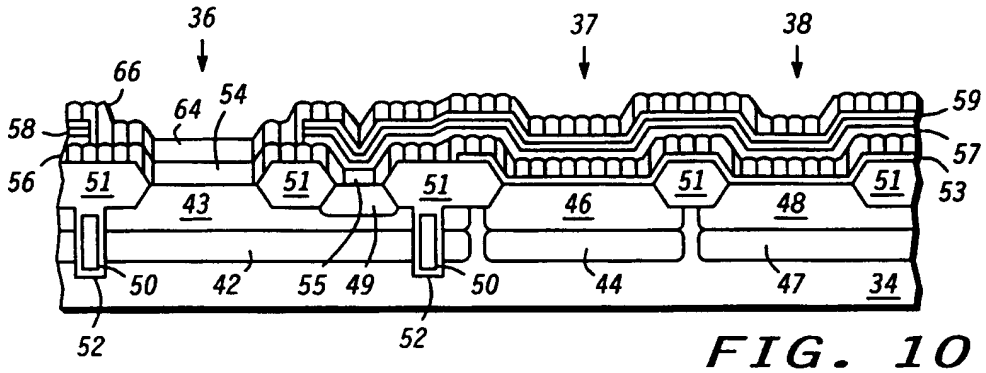


FIG. 10

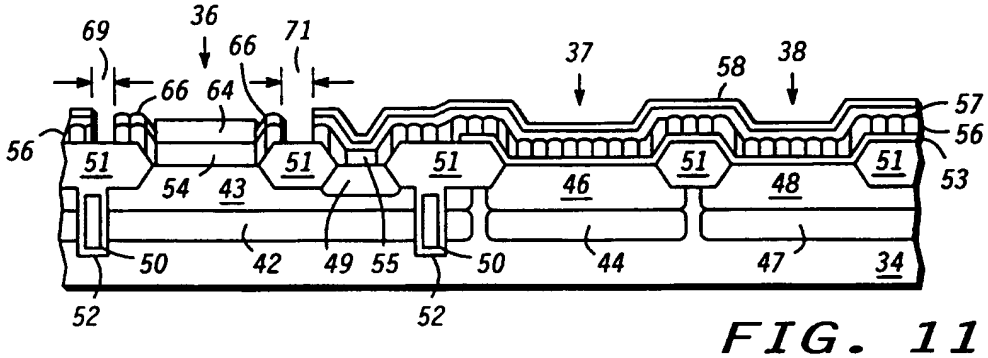


FIG. 11

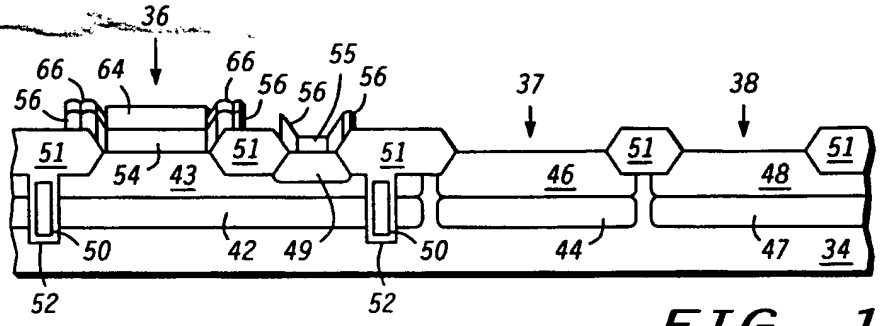


FIG. 12

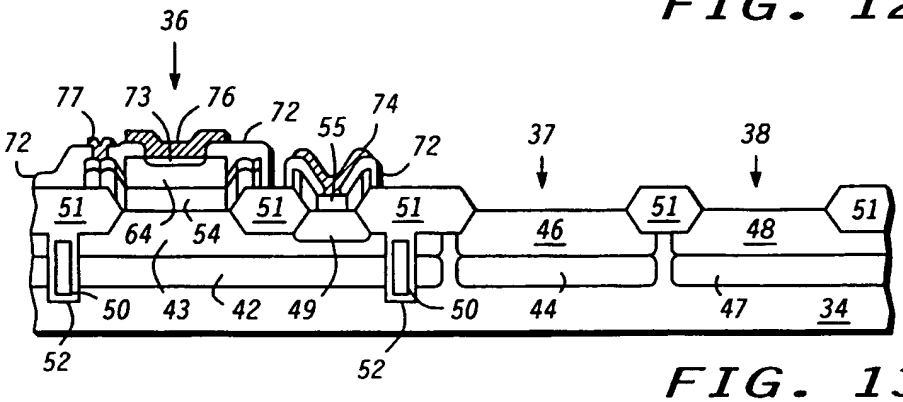


FIG. 13